A Zero-Current-Switched PWM Full Bridge DC-DC Converter

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***Abstract*—In this paper a full bridge isolated DC-DC converter is proposed where the active switches are zero-current-switched (ZCS) for the entire range of operation. The proposed converter is targeted for high voltage, high power applications where input side bridge employs insulated gate bipolar field effect transistors (IGBT) and zero voltage turn OFF (ZVS) can not be fully realised due to the tail current of the IGBT. The input side bridge has three half-bridge legs followed by two high frequency transformers. The Net output of the transformers is fed to a diode bridge feeding a resistive load through a LC filter. In contrast to the conventional phase shifted full bridge converter (PSFB), during the zero state (when there is no active power transfer from input to output), current does not circulate in the input bridge as well as in the transformers. Also the converter has low duty cycle loss. Thus the converter is suitable for the applications with wide output voltage variation as well. The proposed circuit also ensures soft commutation of the diode bridge rectifier. The converter operation principle is discussed. A 1.5 kW prototype is built and tested. Key experimental results are presented to verify the operation.**

***Index Terms*—Full bridge, DC-DC converter, zero voltage switching (ZVS), zero current switching (ZCS), IGBT**

I. Introduction

Full bridge DC-DC converter based on phase-shift modulation (PSFB) is widely used in medium power range (few kW to few tens of kW) for its attractive features like achieving zero voltage switching (ZVS) of primary bridge switches at rated load using device capacitance and transformer leakage, high utilization of the transformer, soft-commutation of the diode bridge. But the problems associated with the conventional PSFB are 1) limited and narrow ZVS range. 2) A large inductance in series with the transformer is needed to increase the ZVS range which results in increased voltage stress of secondary diodes and large duty cycle loss. 3) At very light load or no load, ZVS of primary switches can not be maintained. 4) The free-wheeling current in transformer and primary bridge in zero state increases power loss.

In literature, several techniques are proposed to resolve these problems. In [1], two additional switches and one inductor is used in the primary to achieve ZVS over entire load range. An auxiliary resonant circuit consists of two inductors and one capacitor connected between two poles of the primary bridge is proposed in [2] to extend the ZVS range. In [3]–[5], two transformer based solutions are reported. In [3], transformer magnetising inductor helps to increase ZVS range. In [4], two transformers, two capacitors and one inductor are used in the primary bridge. The stored energy in the auxiliary inductor helps to achieve ZVS in low load operation.

Several active [6] and passive [7]–[12] snubbers are reported in literature to reset the transformer current to zero during zero state to improve the conduction loss of the converter. In [6] a switch in series with a capacitor is used in the secondary after the rectifier. At the beginning of a zero state, the switch is turned ON and the capacitor voltage is applied from secondary to reset the transformer current. In [7], a DC blocking capacitor is used in series with the transformer primary. The capacitor voltage helps to reset the winding current during zero state. In [8]–[12], additional diodes and capacitors are employed in the secondary to reset the primary current. In all of the cases, the reset time depends on the magnitude of the capacitor voltage. High capacitor voltage helps to reset the current quickly but increase the voltage stress on semiconductor devices. Reset of primary current helps to achieve zero current switching (ZCS) of the primary devices.

Zero current switched (ZCS) full bridge converters are widely reported in literature [6], [13], [14]. ZCS techniques are suitable for high power converters where IGBTs are commonly used. Because of the tail current of the IGBT complete ZVS turn OFF can not be achieved [13], [14]. [13] employes an active snubber in the secondary to achieve ZCS of the primary switches. In [14], the primary is a current fed full bridge where active switched capacitor snubber is used.

In this paper a novel ZCS full bridge isolated DC-DC converter with two transformers is presented. An auxiliary half-bridge leg is used in the primary. The proposed topology can be used for applications requiring wide variation of the output voltage. The converter topology with the proposed modulation scheme has following features. (a) The primary full-bridge is zero current switched (ZCS). The auxiliary switches are turned ON with zero current (ZCS) and turned OFF with zero voltage (ZVS). The proposed topology is suitable for high power converters with IGBT modules. (b) ZCS is independent of output load variation. The converter is soft-switched for entire range of operation. (c) The converter has low duty cycle loss compared to conventional ZVS PSFB converter, (d) In the zero state, the converter has no circulating current in the

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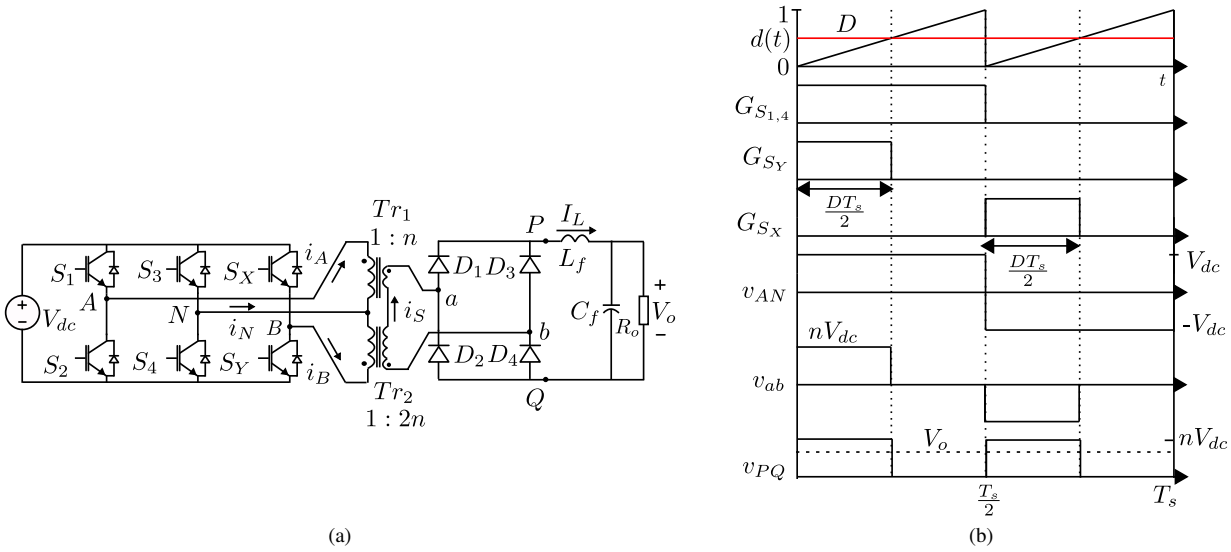


(a) (b)

Fig. 1: (a) Proposed DC-DC converter, (b) Gating signals of the primary switches.

primary bridge as well as in the transformers. To reset the transformer currents the input DC voltage is used. It does not require additional capacitances and hence avoids associated voltage stress. (e) The modulation ensures soft commutation of secondary diode bridge resulting in reduced loss.

The organisation of this paper is as follows. Section II presents the modulation strategy of the converter. Steady state operation and soft-switching process are discussed in section III. The key experimental results verifying the converter operation are presented in section IV.

II. Proposed Converter and Modulation Strategy

The proposed DC-DC converter is shown in Fig. 1a. In the input side, the converter has full-bridge structure ($S_1 - S_4$) along with an auxiliary half-bridge leg ($S_X - S_Y$). The converter has two high frequency transformers (HFT), Tr_1 and Tr_2 with turns ratios $1:n$ and $1:2n$ respectively. The secondary windings are series connected and feeding a full-bridge rectifier as seen in Fig. 1a. The output of the rectifier is connected to a resistive load through a LC filter.

The switch pairs $S_1 - S_2$ and $S_3 - S_4$ are complementary switched with a dead time between their gating signals. The gating signals of S_1 and S_4 ($G_{S_{1,4}}$) are square waves with duty ratio 0.5 and period T_s, as seen in Fig. 1b. The gating signals of S_2 and S_3, $G_{S_{2,3}} = \overline{G}_{S_{1,4}}$. A unipolar sawtooth carrier with period $\frac{T_s}{2}$ is compared with the voltage reference signal $d(t)$ to generate the gating signals of S_X and S_Y as shown in Fig. 1b. The magnitude of the reference signal, D, varies between $[0, 1]$. The modulation scheme applies a high frequency AC voltage v_{ab} with voltage levels $\pm nV_{dc}$ and 0, at the input of the secondary rectifier. The high frequency AC is rectified by the secondary diode bridge $D_1 - D_4$. The rectifier output voltage, v_{PQ}, is shown in Fig. 1b. v_{PQ} has voltage levels nV_{dc} and 0. By applying, volt-second balance across the filter inductor L_f, output voltage V_o is given by (1).

$$V_o = nDV_{dc} \tag{1}$$

III. Steady State Operation and Analysis

In this section, the steady state operation of the converter is analysed considering primary bridge device parasitic capacitance C_s and transformer leakage inductances. L_{lks_1} and L_{lks_2} are the leakage inductances of Tr_1 and Tr_2 respectively seen from the transformer secondary terminals and $L_{lks} = L_{lks_1} + L_{lks_2}$. For the ease of analysis, the output current of the secondary diode bridge I_L is considered to be ripple free over a switching cycle (T_s) and is modelled as current sink. What follows is a detailed discussion of the converter switching process over one half of the switching cycle, T_s. The operation in the other half cycle is similar. Switching waveforms are shown in Fig. 3a.

A. Mode 1 ($t_0 < t < t_1$, Fig. 2)

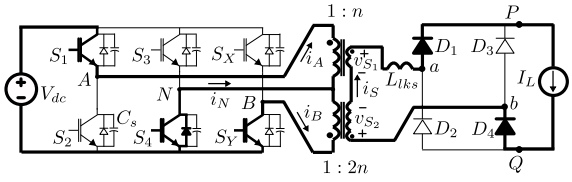


Fig. 2: Circuit configuration in Mode 1.

In this interval the switches S_1, S_4 and S_Y are ON. Hence, the applied primary voltages are $v_{AN} = V_{dc}$ and $v_{BN} = 0$.

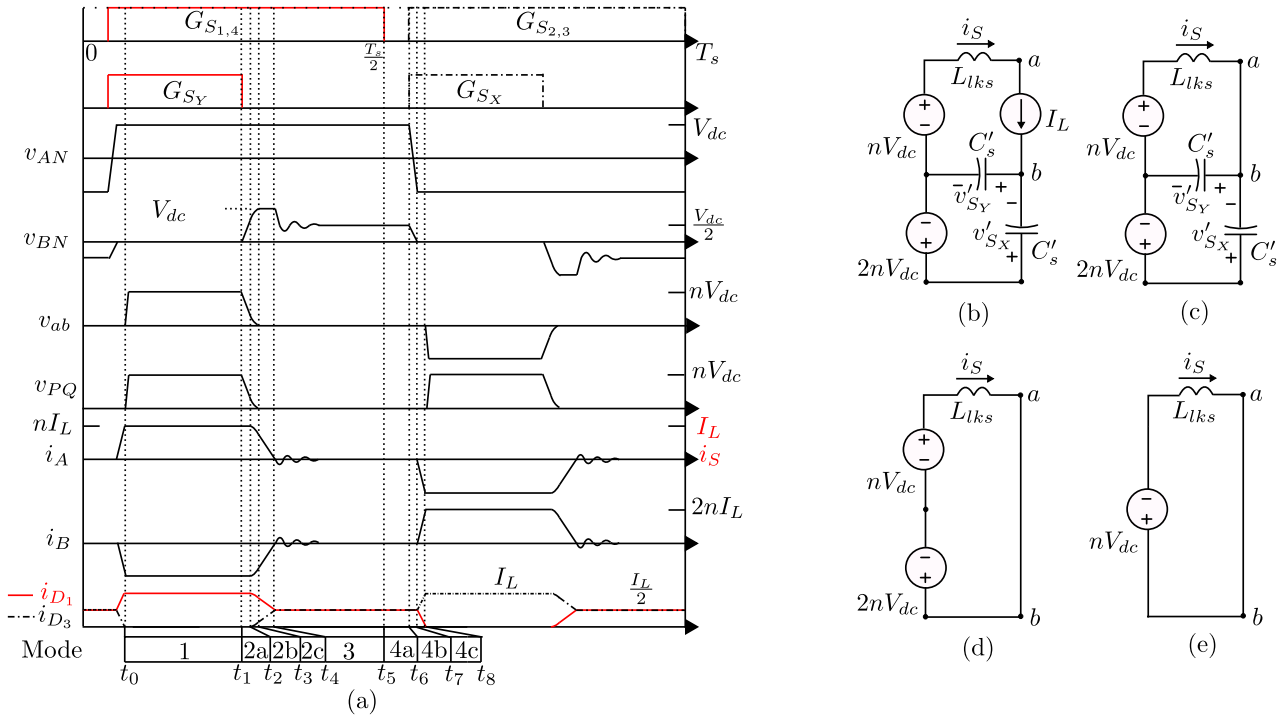


Fig. 3: (a) Switching waveforms over T_s considering circuit parasitics. Equivalent circuit in- (b) Mode 2a, (c) Mode 2b, (d) Mode 2c and (e) Mode 4c.

From the transformer relationship and applying KCL at node N following equations can be obtained.

$$\begin{aligned} i_A + i_B + i_N &= 0 \\ i_A &= n i_S \\ i_B &= -2n i_S \\ v_{T_1} &= n v_{AN} \\ v_{T_2} &= 2n v_{BN} \end{aligned} \tag{2}$$

$i_{A,B}$ are the transformer primary currents and i_S is the secondary current. v_{T_1} and v_{T_2} are secondary voltages of Tr_1 and Tr_2 respectively (Fig. 2). In this mode, the rectifier input voltage and current are given in (3).

$$\begin{aligned} v_{ab} &= v_{T_1} - v_{T_2} = nV_{dc} \\ i_S &= I_L \end{aligned} \tag{3}$$

Diodes D_1, D_4 are conducting I_L. Active power is transferred from source to load.

B. Mode 2 ($t_1 < t < t_4$)

This mode starts at t_1, when S_Y is turned OFF. Mode 2 has three sub-modes as follows.

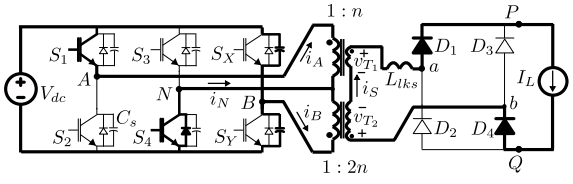


Fig. 4: Circuit configuration in Mode 2a.

1) Mode 2a ($t_1 < t < t_2$, Fig. 4): After t_1, i_B starts charging the capacitance (C_s) of S_Y and discharging the capacitance of S_X. Due to C_s, voltage rise across S_Y is slow and which helps to achieve ZVS turn OFF of S_Y. The equivalent circuit is shown in Fig. 3b. The primary currents are $i_A = nI_L$ and $i_B = -2nI_L$. The voltage across S_Y, seen from secondary, can be expressed as (4), where $C'_s = \frac{C_s}{4n^2}$.

$$v'_{S_Y} = \frac{I_L}{2C'_s}(t - t_1) \tag{4}$$

At t_2 when v'_{S_Y} rises to nV_{dc}, this sub-mode ends.

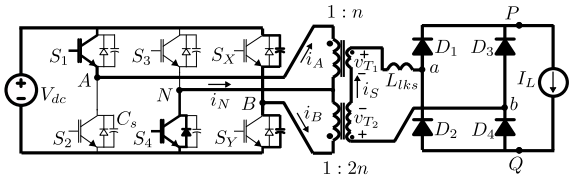


Fig. 5: Circuit configuration in Mode 2b.

2) Mode 2b ($t_2 < t < t_3$, Fig. 5): After t_2 when $v'_{S_Y} > nV_{dc}$, the polarity of the effective voltage applied across L_{lks} is changed (becomes negative). D_2 and D_3 are forward biased. Hence the transformer secondary terminals ab are shorted by the diode bridge. The load current I_L free-wheels through the diode bridge. The equivalent circuit is shown in Fig. 3c. Applying Kirchhoff's laws, following circuit

equations are derived.

$$\begin{aligned} v'_{S_Y} &= nV_{dc} + \omega_r L_{lks} I_L \sin\omega_r(t-t_2) \\ i_A &= ni_S = nI_L \cos\omega_r(t-t_2) \\ i_B &= -2ni_S = -2nI_L \cos\omega_r(t-t_2) \end{aligned} \tag{5}$$

Where $\omega_r = \dfrac{1}{\sqrt{2L_{lks}C'_s}}$. At t_3 when $v'_{S_Y} = 2nV_{dc}$, this sub-mode ends. The capacitance across S_Y is charged to V_{dc} and the capacitance across S_X is completely discharged.

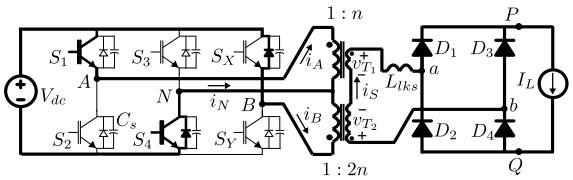


Fig. 6: Circuit configuration in Mode 2c.

3) Mode 2c ($t_3 < t < t_4$, Fig. 6): The anti-parallel diode of S_X is forward biased and starts conducting. The applied primary voltages are $v_{AN} = V_{dc}$ and $v_{BN} = V_{dc}$. The equivalent circuit is shown in Fig. 3d. The winding currents $i_{A,B,S}$ are changed linearly in this interval.

$$\begin{aligned} i_S &= i_S(t_3) - \frac{nV_{dc}}{L_{lks}}(t-t_3) \\ i_A &= ni_S = ni_S(t_3) - \frac{n^2V_{dc}}{L_{lks}}(t-t_3) \\ i_B &= -2ni_S = -2ni_S(t_3) + \frac{2n^2V_{dc}}{L_{lks}}(t-t_3) \end{aligned} \tag{6}$$

This results in soft commutation of secondary diodes (see Fig. 3a). At t_4, the winding currents become zero and this mode ends.

C. Mode 3 ($t_4 < t < t_5$, Fig. 7)

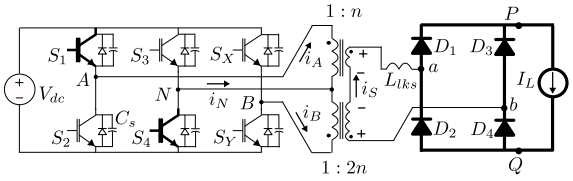


Fig. 7: Circuit configuration in Mode 3.

In the beginning of this mode, the circuit starts resonating with zero initial current. The device capacitances of $S_{X,Y}$ and the transformer leakage inductances take part in the resonance. Due to lossy components of the practical circuit this oscillation dies down quickly and $i_{A,B,S}$ become zero. As the switches S_1 and S_4 are kept ON, the transformer voltage $v_{T_1} = nV_{dc}$. At steady state v_{T_2} has to be nV_{dc} to maintain $i_S = 0$. And thus v_{BN} settles to $\dfrac{V_{dc}}{2}$. At steady state, transformer voltage equation is given by (7).

$$v_{ab} = (nv_{AN} - 2nv_{BN}) = 0 \tag{7}$$

The load current free wheels through the secondary diode bridge only. The primary bridge and the transformers do not conduct in this state. No active power is transferred from source to load.

D. Mode 4 ($t_5 < t < t_8$)

This mode begins at t_5 when S_1 and S_4 are turned OFF. This mode has three sub modes as follows.

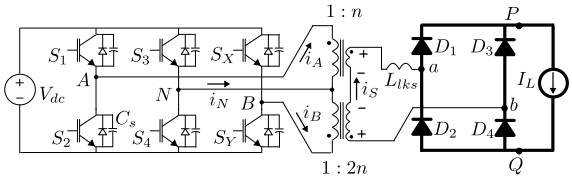


Fig. 8: Circuit configuration in Mode 4a.

1) Mode 4a ($t_5 < t < t_6$, Fig. 8): The turn OFF S_1 and S_4 are zero current (ZCS) transitions as $i_A = i_B = i_N = 0$. The voltage distribution remain same as in Mode 3 (as all pole currents are zero in the primary) i.e. $S_{2,3}$ keep blocking V_{dc} and $S_{X,Y}$ block $\frac{V_{dc}}{2}$.

2) Mode 4b ($t_6 < t < t_7$): At t_6, S_2, S_3 and S_X are turned ON ideally with zero currents (ZCS). But the parasitic capacitances across the devices discharge through these devices quickly, results in some loss. As we have not use any external capacitances, this loss is restricted to small value.

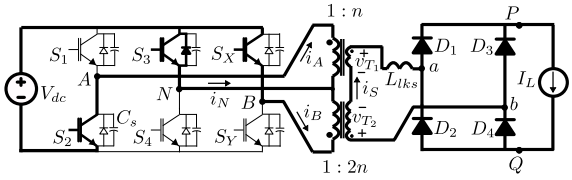


Fig. 9: Circuit configuration in Mode 4c.

3) Mode 4c ($t_7 < t < t_8$, Fig. 9): The equivalent circuit is shown in Fig. 3e. The primary applied voltages are $v_{AN} = -V_{dc}$ and $v_{BN} = 0$. The secondary transformer terminal ab are still shorted through the diode bridge. i_S builds up in the opposite direction as per (8).

$$i_S = -\frac{nV_{dc}}{L_{lks}}(t-t_7) \tag{8}$$

In the diode bridge current transfer between $D_{1,4}$ to $D_{2,3}$ happens linearly. Linear commutation of diode bridge is shown in Fig. 3a. This mode ends at t_8 when $i_S = -I_L$. The diodes $D_{1,4}$ are reverse biased.

Then the circuit enters into next mode shown in Fig. 10. In this mode S_2, S_3 and S_X are ON. The applied primary voltages are $v_{AN} = -V_{dc}$ and $v_{BN} = 0$. In the secondary the rectifier input voltage, $v_{ab} = -nV_{dc}$. Secondary diodes D_2, D_3 are forward biased and carry load current I_L. This is an active state where power flows from input to output and this state is equivalent to Mode 1. Thereafter the converter evolves

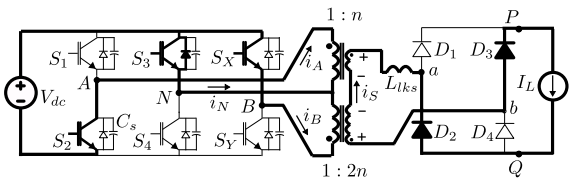
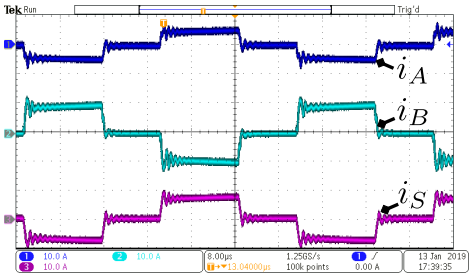
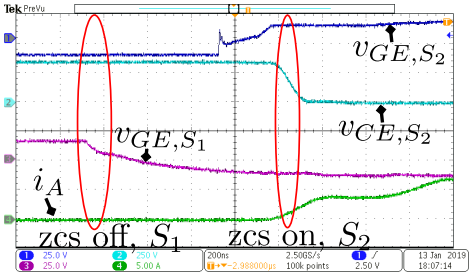


Fig. 10: Circuit configuration in next Mode 1.



(a)



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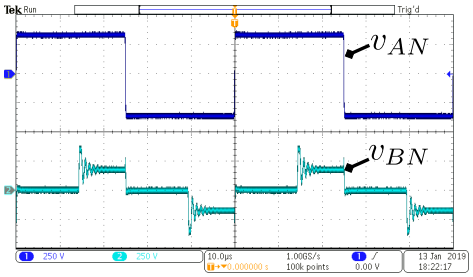
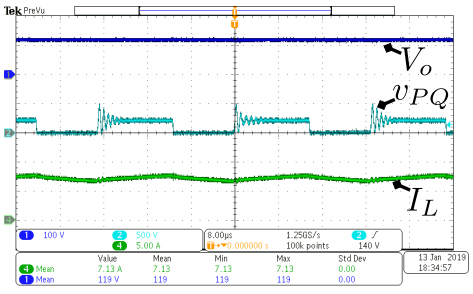


(c)



(d)

Fig. 11: Experimental results- (a) transformer currents, (b) ZCS transitions of $S_1 - S_2$, (c) transformer primary voltages, (d) diode bridge output.

through similar set of modes in the same order as discussed above with other symmetrical switches and diodes.

Neglecting the transition times, the above switching process applies an average voltage over T_s across PQ, $\overline{v}_{PQ} = nDV_{dc}$ which is the desired DC output voltage, V_o (see Fig. 3a).

IV. Experimental Results

The modulation strategy and switching process of the proposed converter are experimentally verified in a 1.5 kW hardware prototype. Table I presents the operating condition. 1200 V, 75 A SEMIKRON IGBT modules SKM75GB123D

TABLE I: Operating condition

DC input (V_{dc})	350V
Output voltage (V_o)	120V
Output power (P_{out})	1.5kW
HFT turns ratio (n)	2/3
Switching frequency ($f_s = \frac{1}{T_s}$)	20kHz

are used in the primary bridge. MEE 75-12DA, IXYS fast recovery diode modules are used in the diode bridge. To drive the IGBT modules, optically isolated gate drivers, ACPL 339J, with driving voltage level $\pm$ 15V, are used. The switching frequency is 20kHz. A 600 ns dead-time is provided between two IGBTs of a half-bridge leg. Ferrite core (E 80/38/20) HFTs with turns ratio 51:34 and 51:68 are used. The leakage inductances of the transformers seen from primary are in the order of 6-8μH. Xilinx Zynq-7000 SoC control platform is used to implement the modulation strategy and to generate gating signals of the IGBTs. key experimental results are presented in Fig. 11.

Fig. 11a shows the transformer primary currents, i_A, i_B and the secondary current i_S. As discussed in section III and shown in Fig. 3a, in zero state transformer winding currents are zero. Hence, unlike the conventional phase shifted full bridge converter, there is no power loss in the primary half bridge legs and in the transformer during the zero state.

Fig. 11b shows the ZCS turn OFF of S_1 and ZCS turn ON of S_2. As seen from the figure, the gating signal of S_1, v_{GE,S_1} is removed when the pole current $i_A = 0$. Which also indicates that the switch current is zero during the turn OFF transition of S_1 and hence the turn OFF loss of the IGBT due to long tail current is avoided here.

As seen from Fig. 11b, the gating signal of S_2, v_{GE,S_2} is applied and collector-emitter voltage v_{CE,S_1} falls to zero. The pole current i_A then slowly rises to the steady state value, $nI_L = 8.33$A. Hence S_2 is turned ON with zero current.

Transformer primary voltages, v_{AN} and v_{BN} are shown in Fig. 11c. v_{AN} has voltage levels $\pm$350V. v_{BN} has voltage levels $\pm V_{dc} = \pm$350V, $\pm\frac{V_{dc}}{2} = \pm$175V and 0. This result verifies the operation of the primary bridge and matches with the analytical waveforms presented in Fig. 3a.

Output voltage V_o, output current I_L and the pole voltage v_{PQ} are shown in Fig. 11d. The output voltage V_o is ripple free with magnitude 120 V. I_L has low ripple with average value 12.5 A. v_{PQ} has voltage levels $nV_{dc} = 233.3$ V and 0.

Like in a conventional PSFB converter, the voltage oscillation observed in v_{PQ} is due to the resonance the diode parasitic capacitances with transformer leakage inductances after the zero to active state transition.

V. Conclusion

This paper demonstrates a novel full bridge isolated DC-DC converter topology. The converter employs one auxiliary half bridge leg and an additional transformer to achieve the following goals. The zero current (ZCS) turn ON of all active switches of the primary bridge are ensured. ZCS turn OFF of the switches in two legs are achieved. The auxiliary leg switches are turned off with zero voltage. ZCS turn OFF mitigates the turn OFF loss of the IGBTs due to long tail current. The auxiliary leg and the transformer reset the primary winding currents during zero state. Hence, the primary bridge and the transformers do not incur any loss during zero state. The ZCS of the switches are achieved over the full range of converter operation without using large series inductances in series with the transformer windings. This results in low duty loss compared to a conventional PSFB with large series inductance to support wide ZVS range. A Detailed discussion on converter operation showing different switching modes is presented. Key experimental results are given to verify the operation of the proposed converter.

References

[1] J. G. Cho, J. A. Sabate, and F. C. Lee, "Novel full bridge zero-voltage-transition pwm dc/dc converter for high power applications," in *Applied Power Electronics Conference and Exposition, 1994. APEC'94. Conference Proceedings 1994., Ninth Annual*. IEEE, 1994, pp. 143–149.

[2] A. Safaee, P. Jain, and A. Bakhshai, "A zvs pulsewidth modulation full-bridge converter with a low-rms-current resonant auxiliary circuit," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4031–4047, 2016.

[3] G.-B. Koo, G.-W. Moon, and M.-J. Youn, "Analysis and design of phase shift full bridge converter with series-connected two transformers," *IEEE Transactions on power electronics*, vol. 19, no. 2, pp. 411–419, 2004.

[4] M. Borage, S. Tiwari, S. Bhardwaj, and S. Kotaiah, "A full-bridge dc–dc converter withzero-voltage-switching overthe entire conversion range," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1743–1750, 2008.

[5] I.-O. Lee and G.-W. Moon, "Soft-switching dc/dc converter with a full zvs range and reduced output filter for high-voltage applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 112–122, 2013.

[6] J.-G. Cho, C.-Y. Jeong, and F. C. Lee, "Zero-voltage and zero-current-switching full-bridge pwm converter using secondary active clamp," *IEEE Transactions on Power Electronics*, vol. 13, no. 4, pp. 601–607, 1998.

[7] J.-G. Cho, J. A. Sabate, G. Hua, and F. C. Lee, "Zero-voltage and zero-current-switching full bridge pwm converter for high-power applications," *IEEE Transactions on Power Electronics*, vol. 11, no. 4, pp. 622–628, 1996.

[8] J.-G. Cho, J.-W. Baek, C.-Y. Jeong, and G.-H. Rim, "Novel zero-voltage and zero-current-switching full-bridge pwm converter using a simple auxiliary circuit," *IEEE Transactions on Industry Applications*, vol. 35, no. 1, pp. 15–20, 1999.

[9] E.-S. Kim, K.-Y. Joe, M.-H. Kye, Y.-H. Kim, and B.-D. Yoon, "An improved soft-switching pwm fb dc/dc converter for reducing conduction losses," *IEEE Transactions on Power Electronics*, vol. 14, no. 2, pp. 258–264, 1999.

[10] J.-G. Cho, J.-W. Baek, C.-Y. Jeong, D.-W. Yoo, and K.-Y. Joe, "Novel zero-voltage and zero-current-switching full bridge pwm converter using transformer auxiliary winding," *IEEE Transactions on Power Electronics*, vol. 15, no. 2, pp. 250–257, 2000.

[11] E.-S. Kim and Y.-H. Kim, "A zvzcs pwm fb dc/dc converter using a modified energy-recovery snubber," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 1120–1127, 2002.

[12] X. Wu, X. Xie, J. Zhang, R. Zhao, and Z. Qian, "Soft switched full bridge dc–dc converter with reduced circulating loss and filter requirement," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1949–1955, 2007.

[13] J. Zhang, X. Xie, X. Wu, G. Wu, and Z. Qian, "A novel zero-current-transition full bridge dc/dc converter," *IEEE transactions on power electronics*, vol. 21, no. 2, pp. 354–360, 2006.

[14] X. Zhang, H. S.-h. Chung, X. Ruan, and A. Ioinovici, "A zcs full-bridge converter without voltage overstress on the switches," *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 686–698, 2010.